

The diagram illustrates a power factor correction (PFC) converter circuit, labeled 1. The input voltage is  $V_{in}$  and the input current is  $I_{in}$ . The output voltage is  $V_{out}$  and the output current is  $I_{out}$ . The circuit includes a power source 2, a differential amplifier 23, a PWM comparator 25, an oscillator 24, a duty limit signal generating circuit 26, and a pulse width control circuit 33. The differential amplifier 23 has a non-inverting input (+) connected to a reference voltage source 22 and an inverting input (-) connected to the output of the PWM comparator 25. The PWM comparator 25 has a non-inverting input (+) connected to the output of the duty limit signal generating circuit 26 and an inverting input (-) connected to the output of the pulse width control circuit 33. The pulse width control circuit 33 includes an on drive circuit 31 and an off drive circuit 32. The on drive circuit 31 is connected to the gate of a MOSFET 11, and the off drive circuit 32 is connected to the gate of a diode 12. The MOSFET 11 is connected to the input voltage  $V_{in}$  and the output voltage  $V_{out}$ . The diode 12 is connected to the output voltage  $V_{out}$  and the input voltage  $V_{in}$ . The output voltage  $V_{out}$  is also connected to a load 3. The circuit also includes a capacitor  $C1$ , an inductor  $L1$ , and resistors  $R11$  and  $R12$ . The output voltage  $V_{out}$  is also connected to a reference voltage source 22. The circuit is labeled 13.

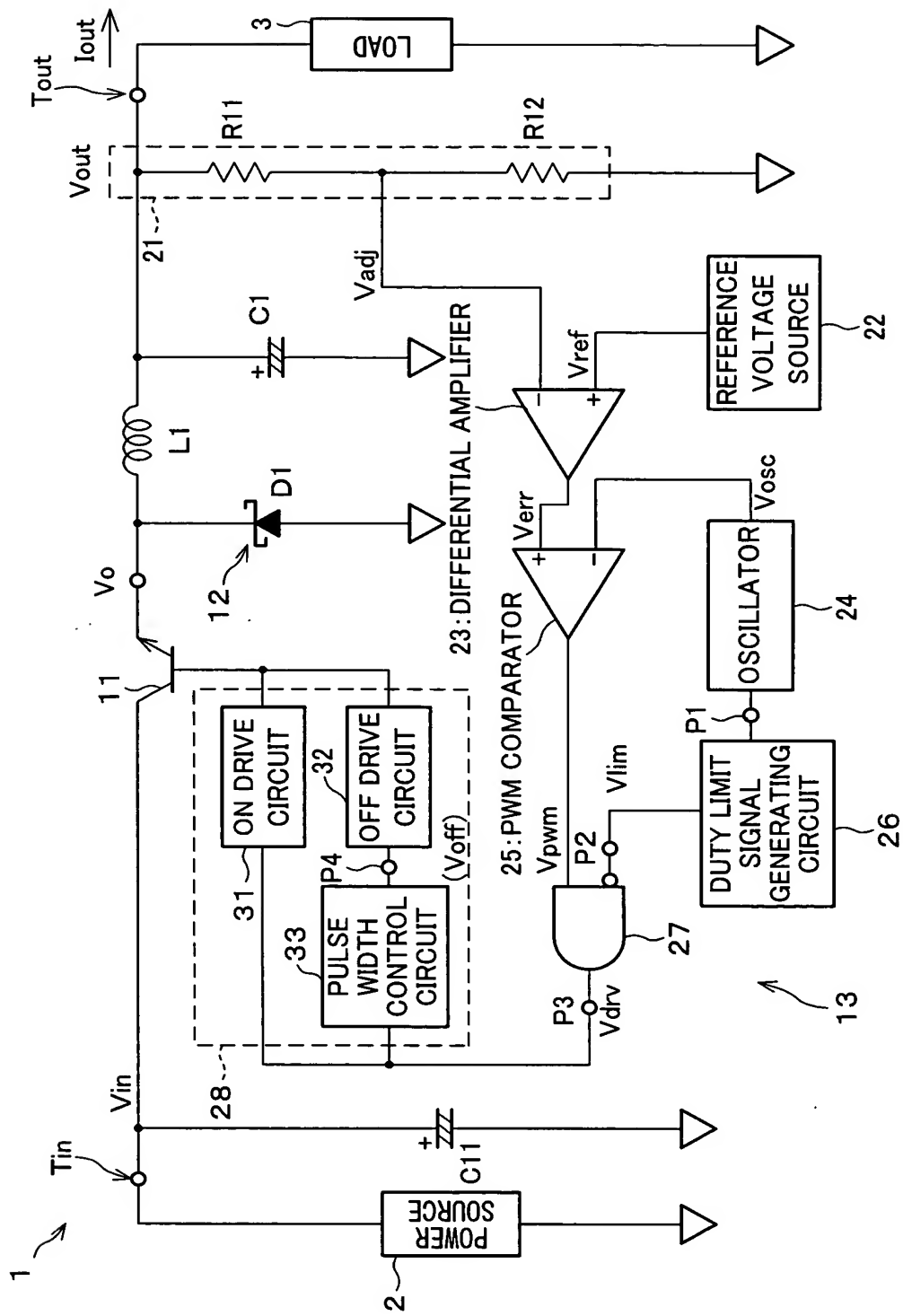


FIG. 2

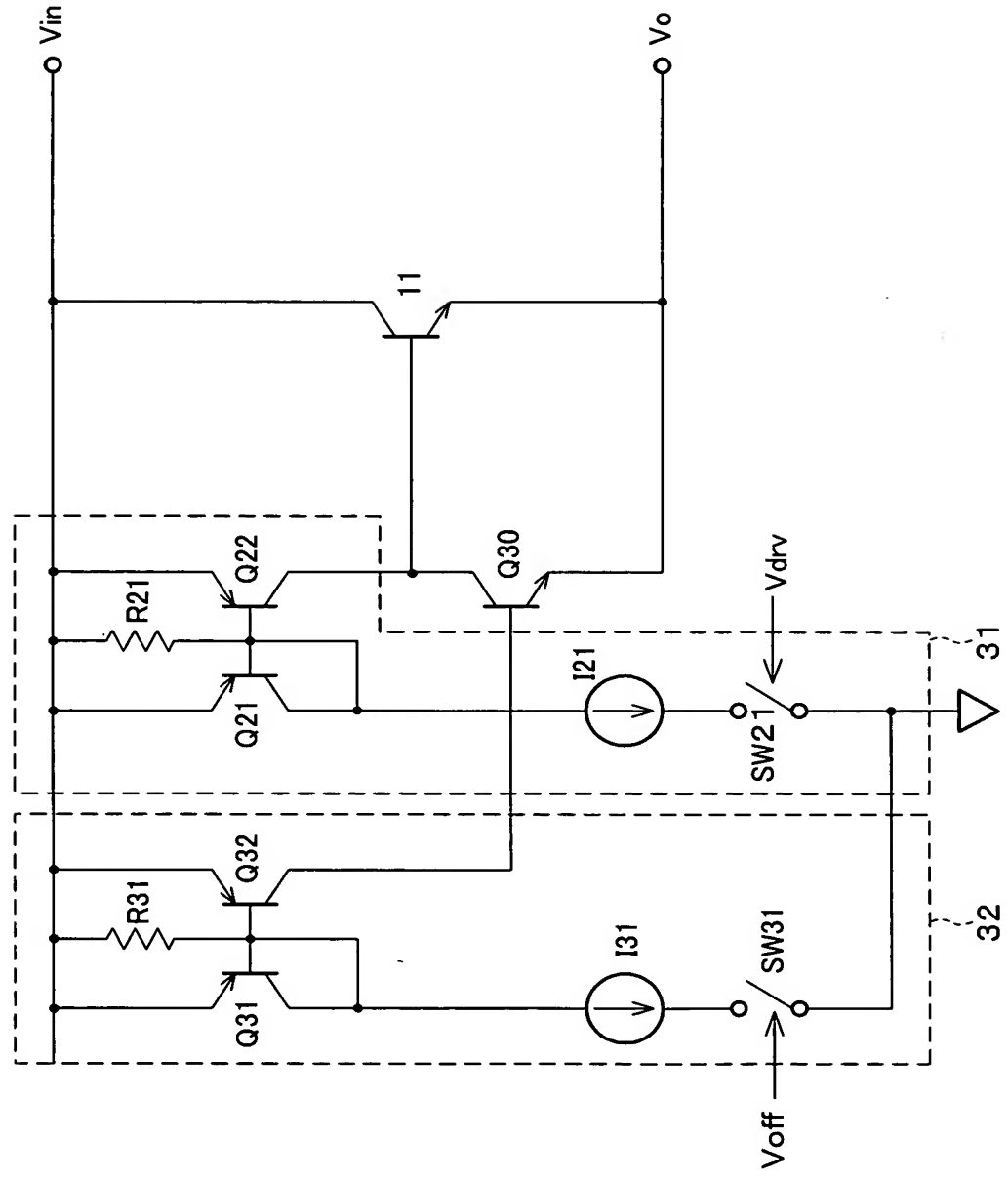
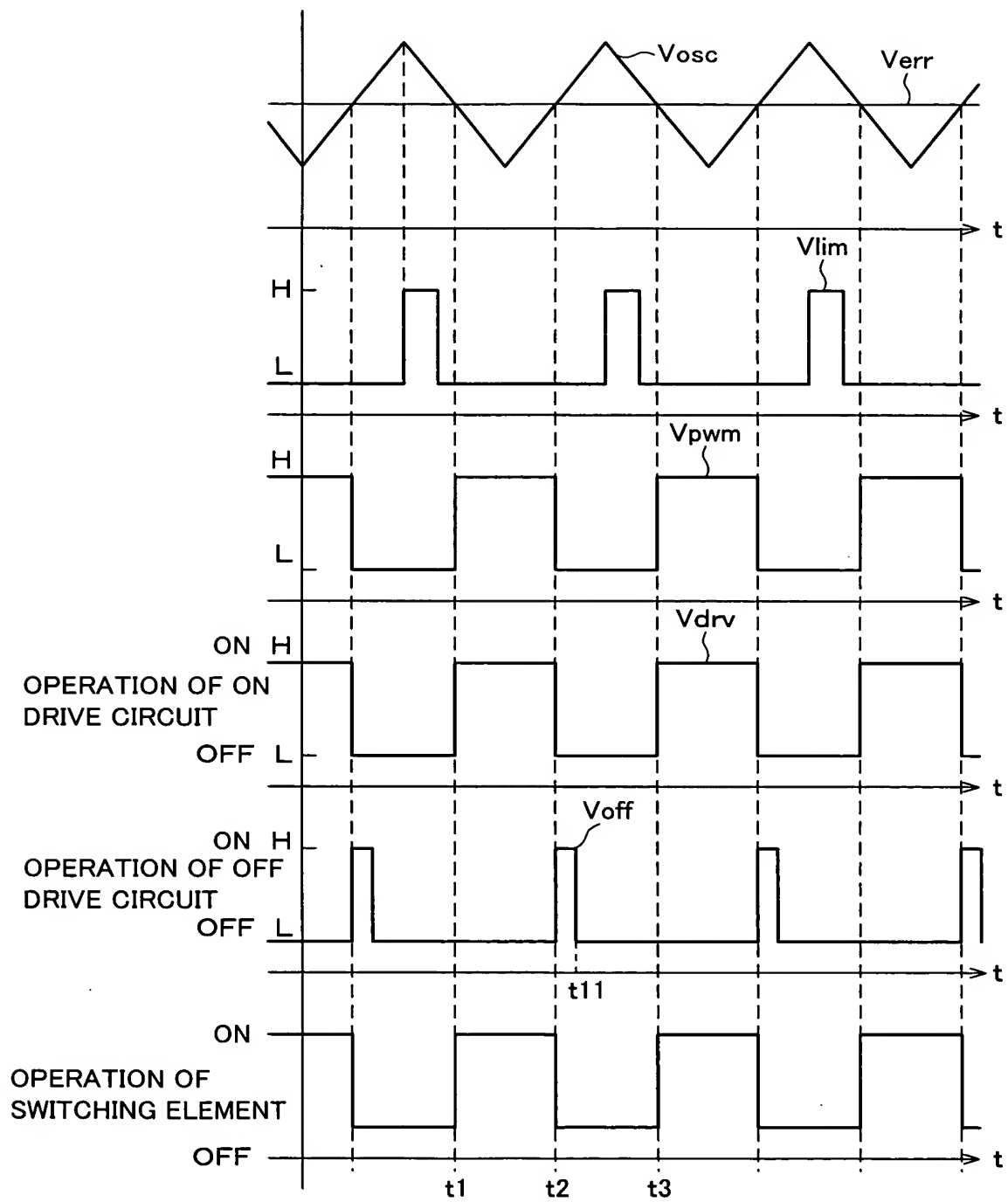


FIG. 3



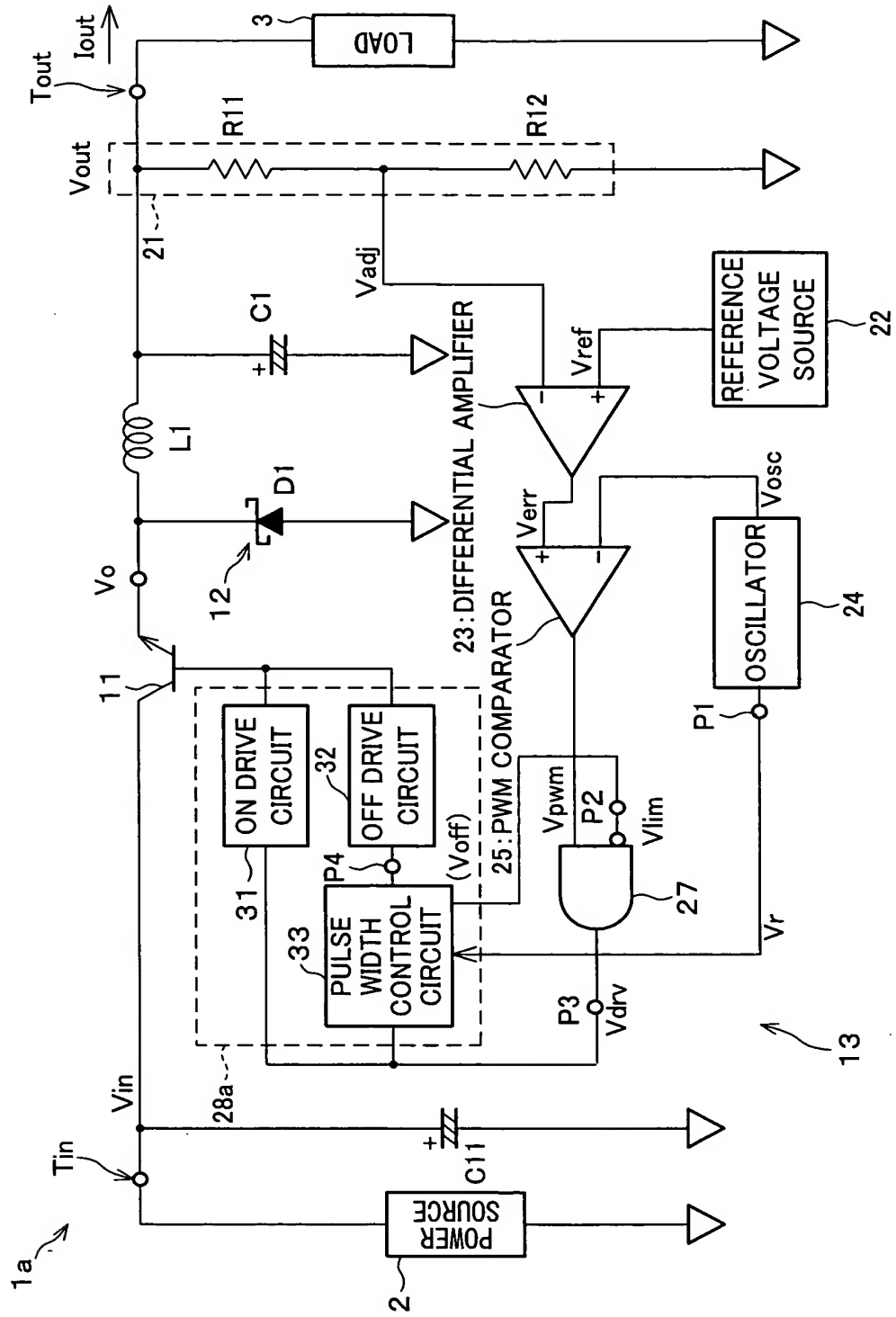


FIG. 5

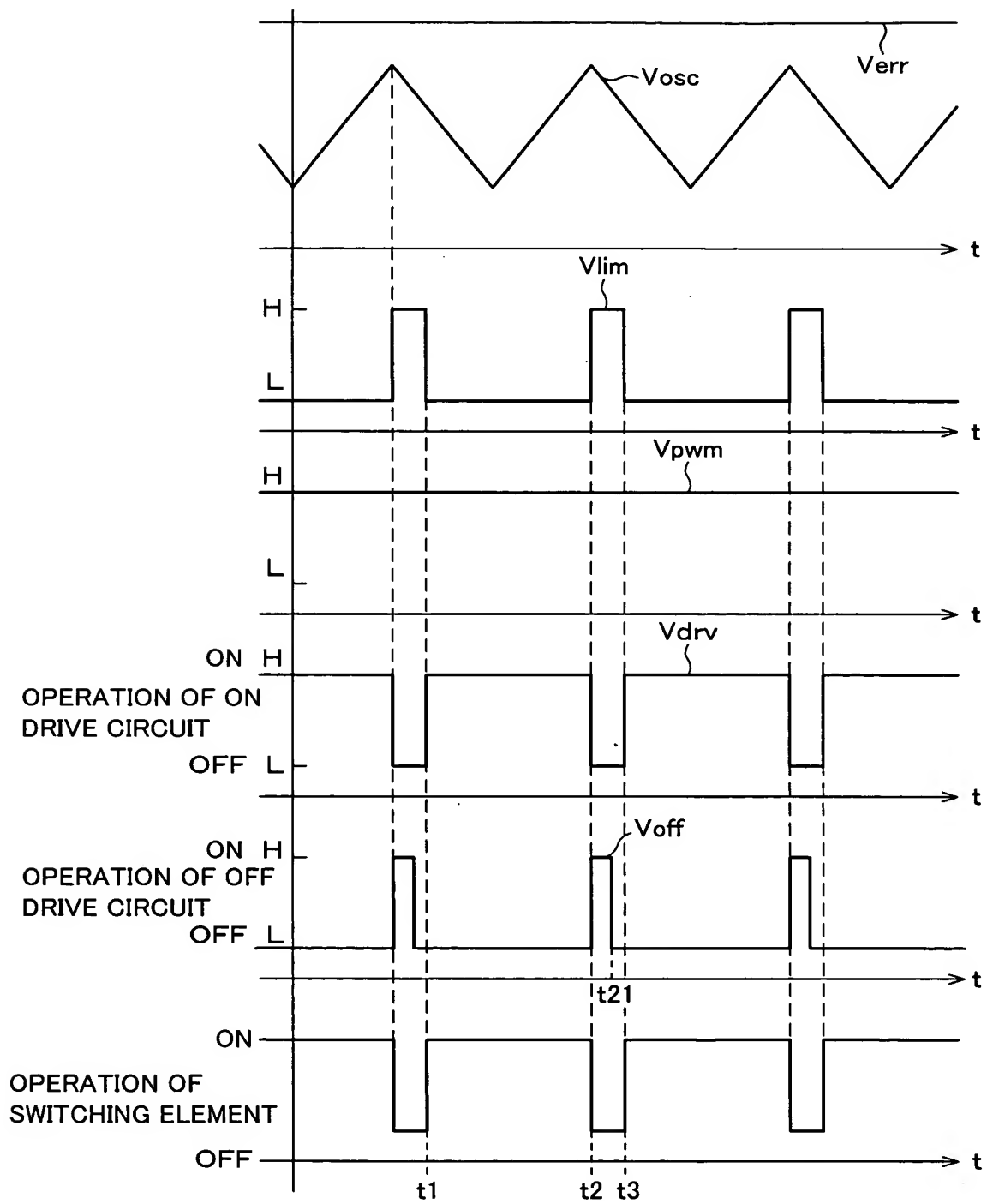
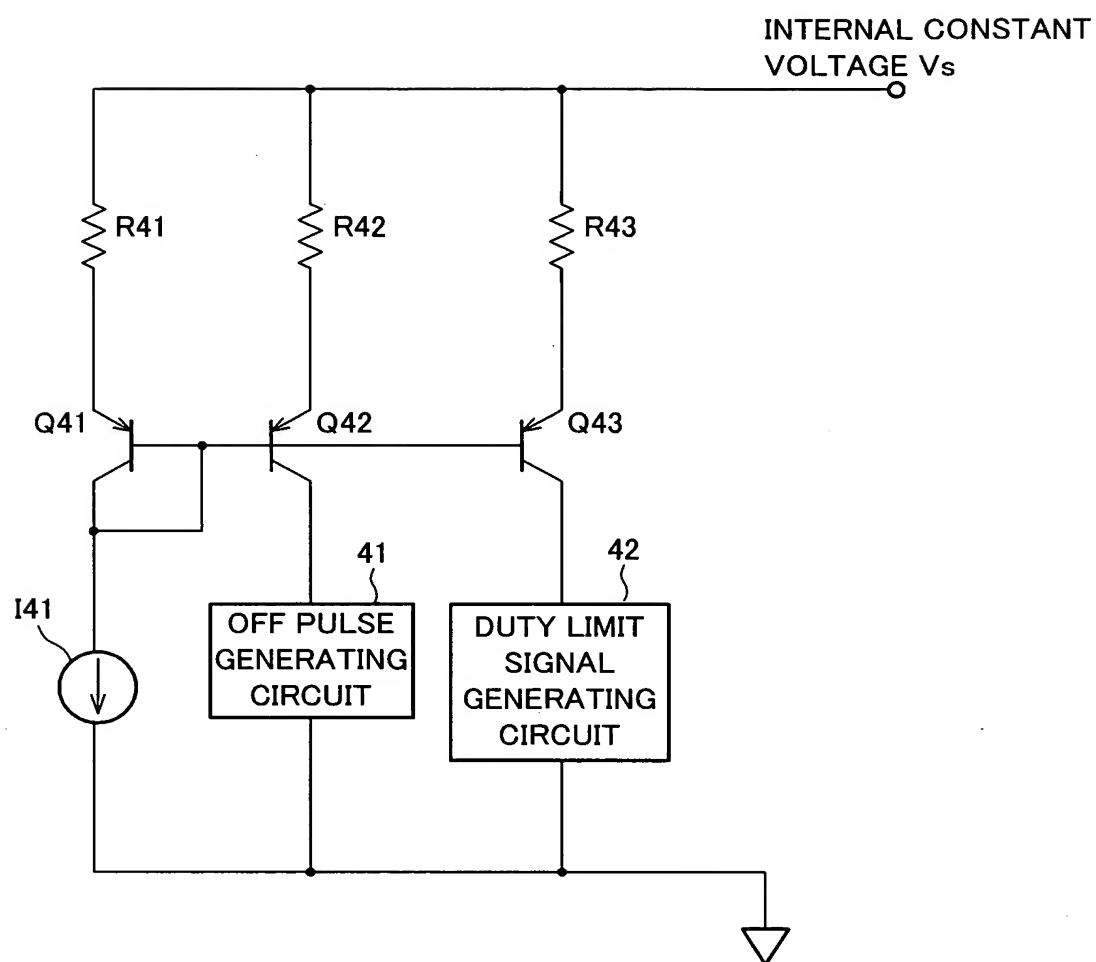


FIG. 6



**FIG. 7**

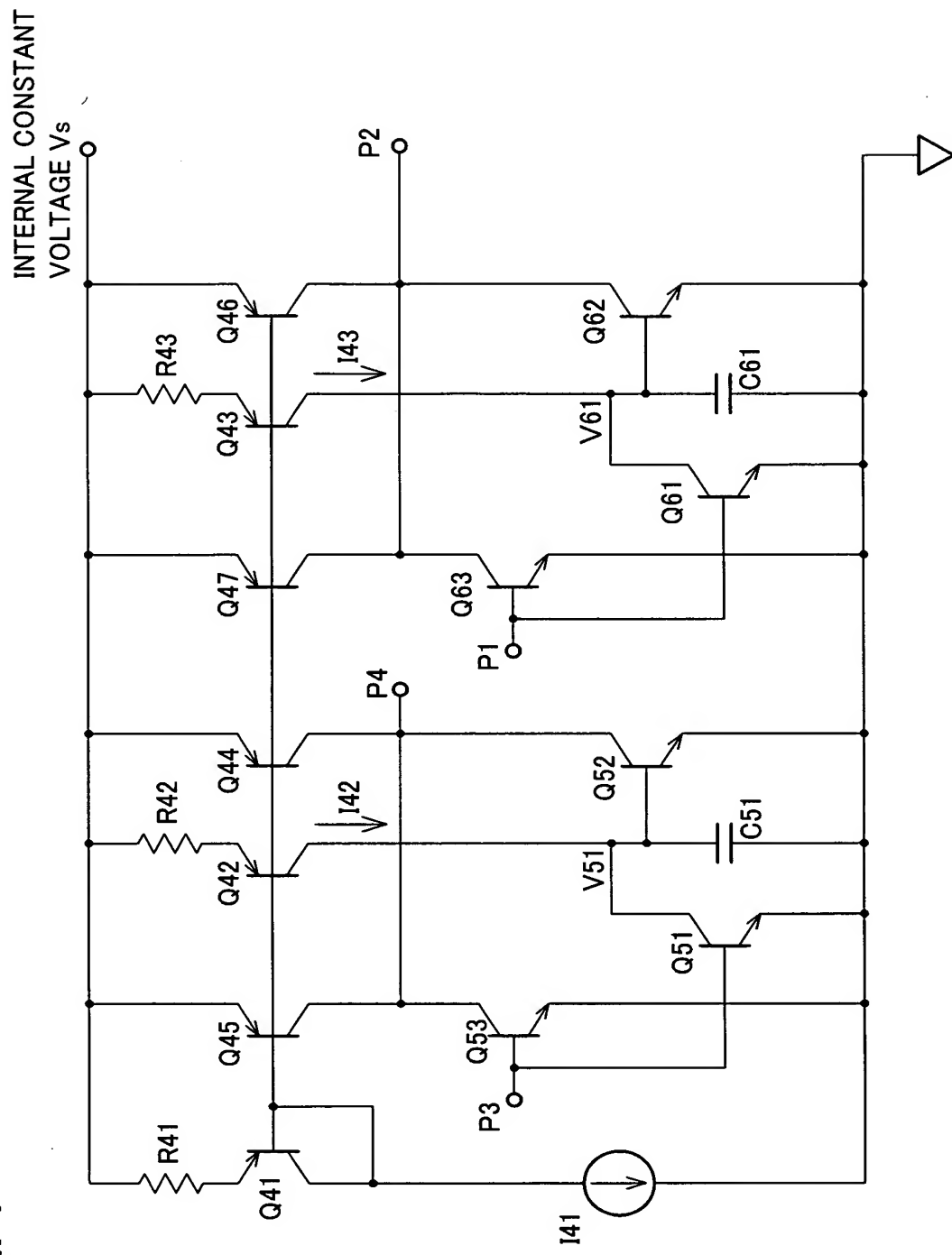


FIG. 8

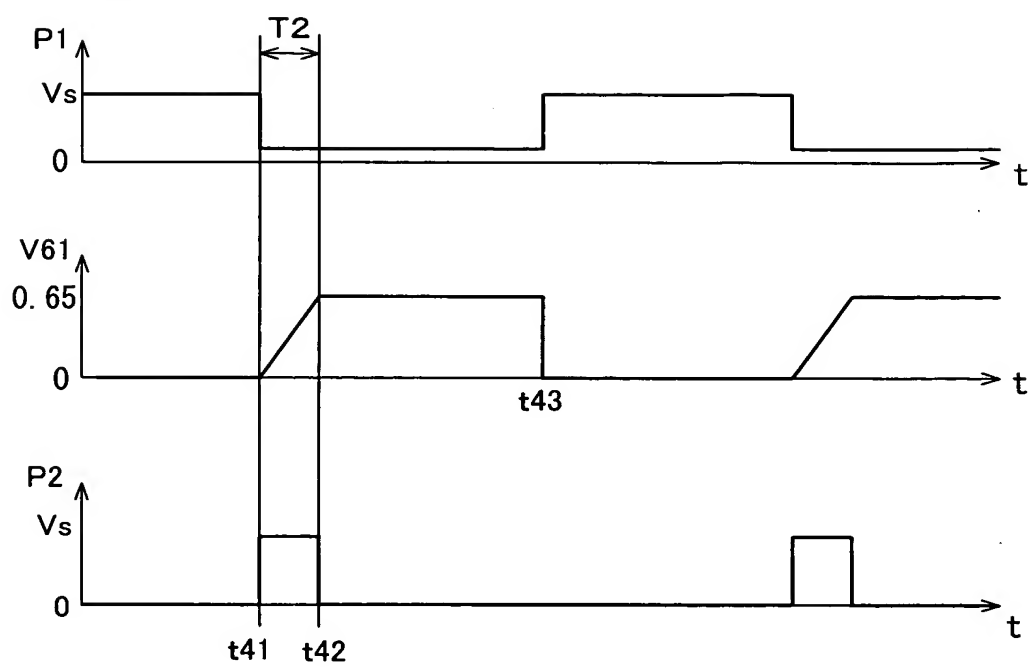


FIG. 9

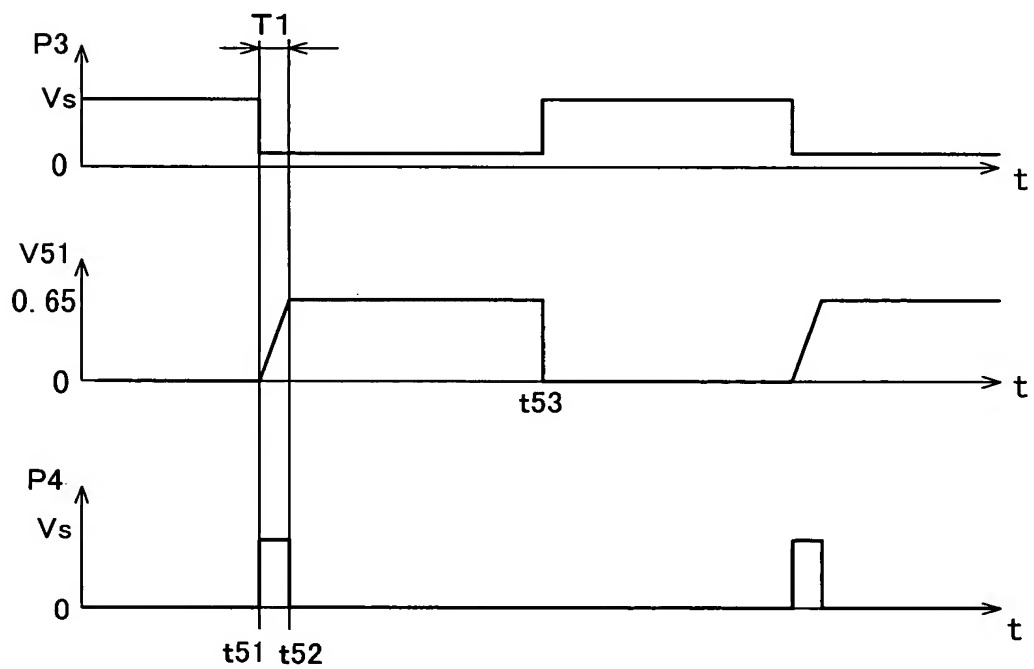
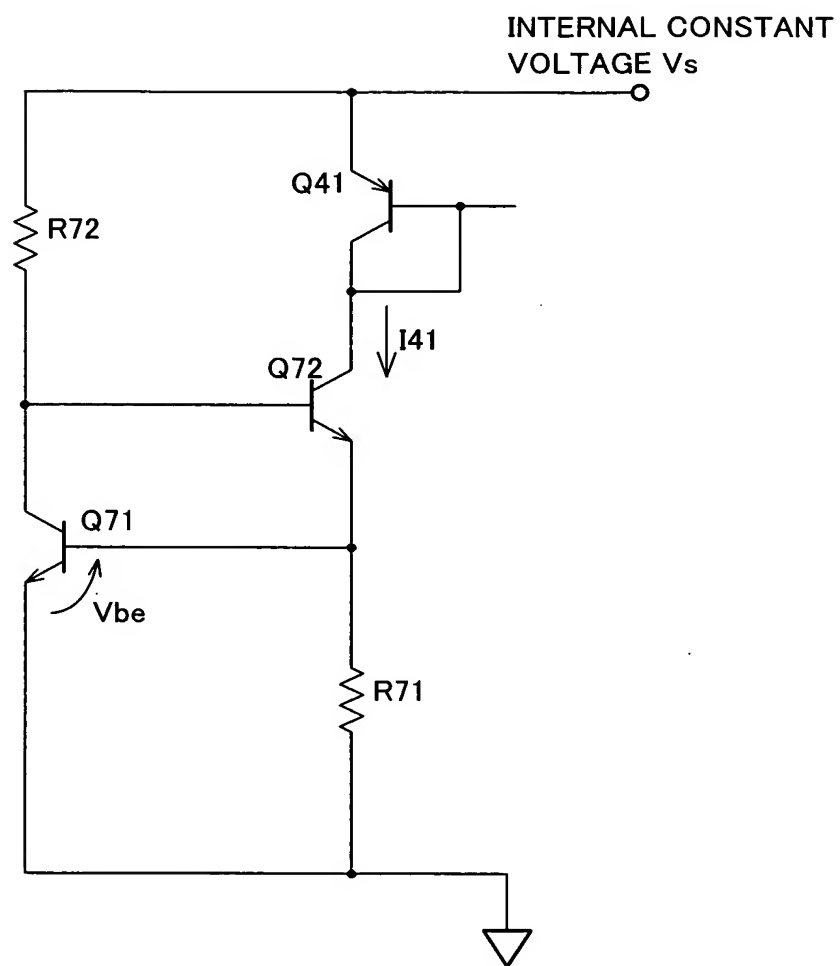




FIG. 10



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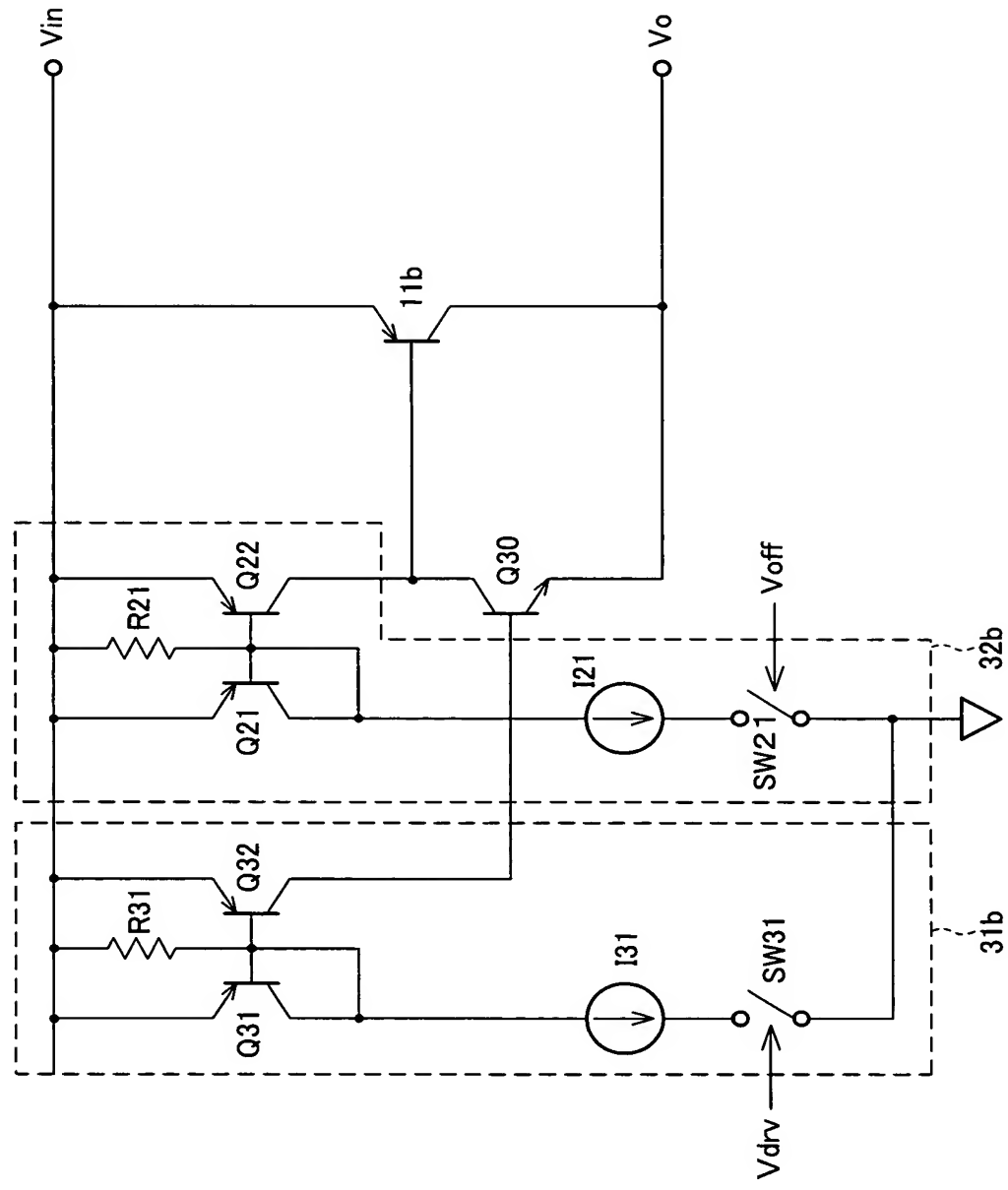


FIG. 12

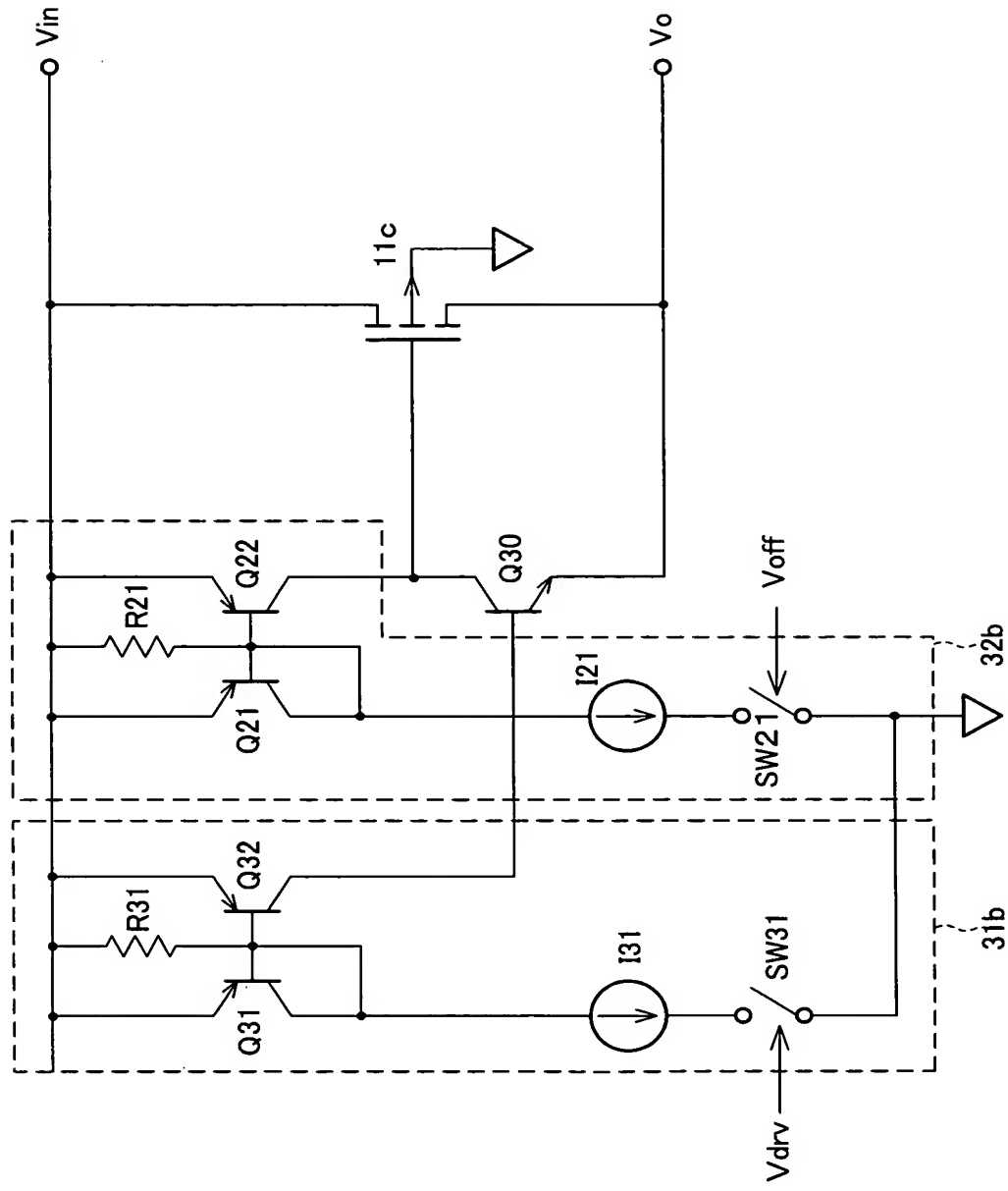


FIG. 13

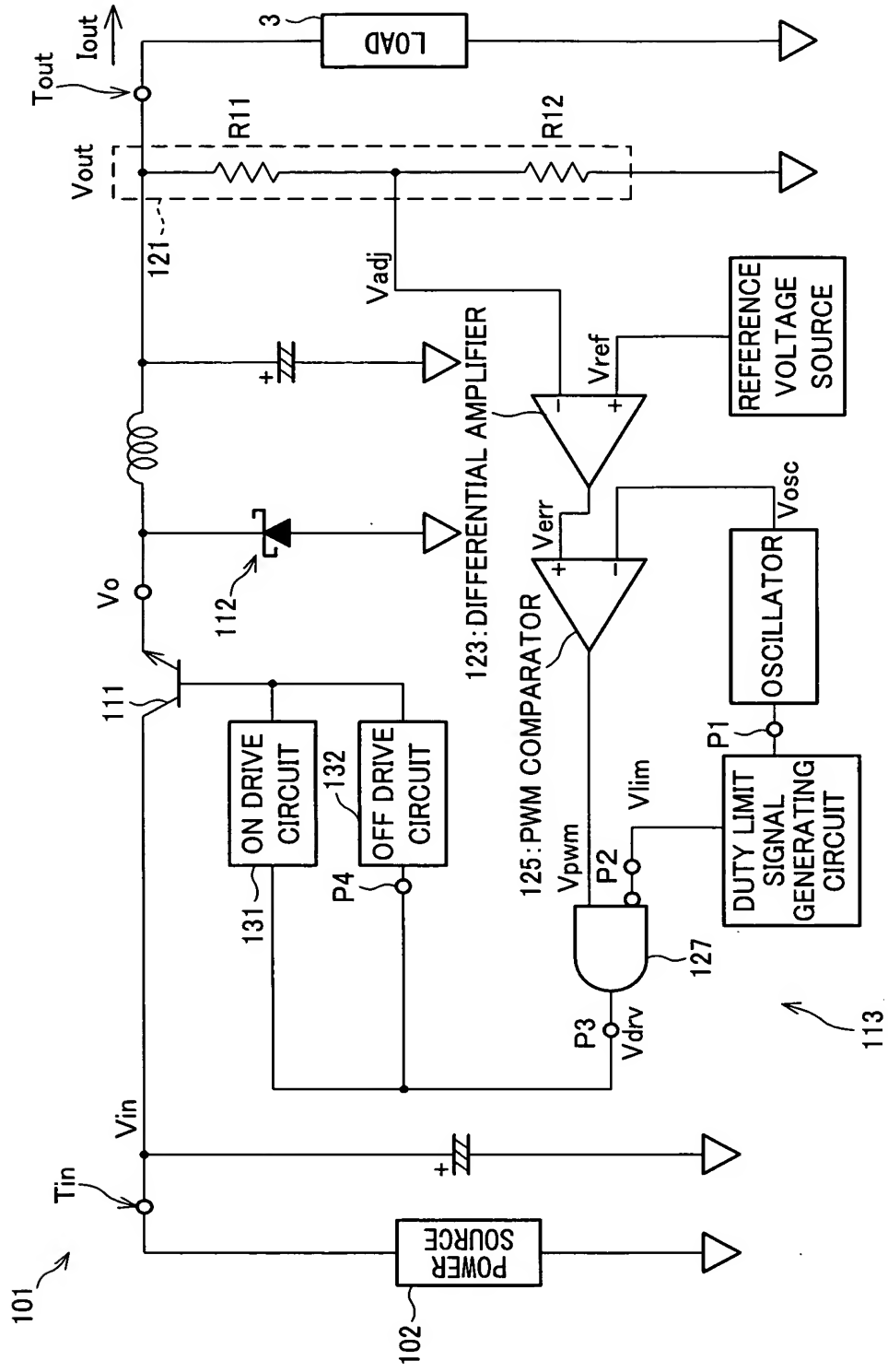


FIG. 14

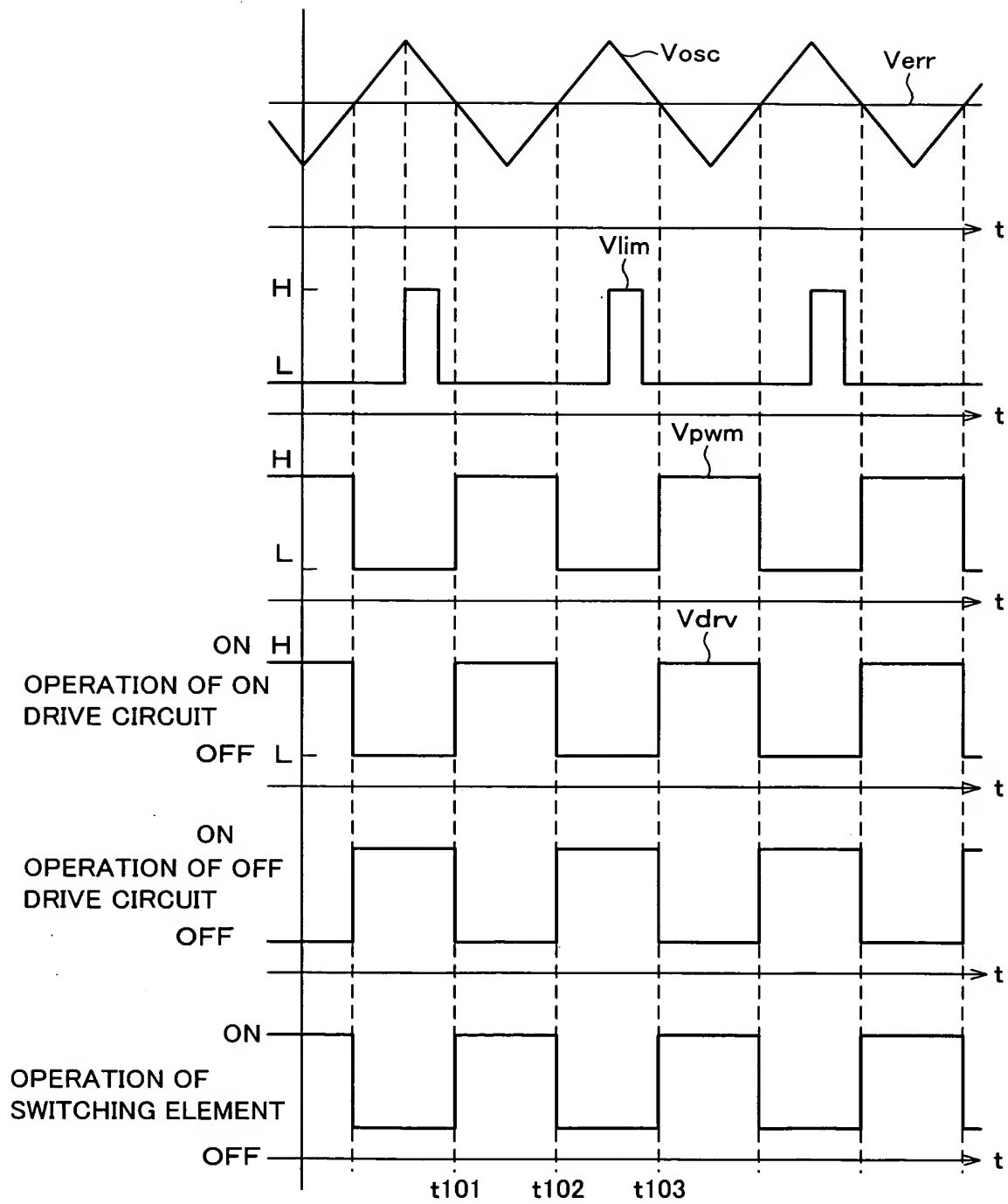


FIG. 15

